White Paper

C-PHY vs D-PHY – Choosing the right signal interface for MIPI Camera and Imaging

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MIPI Camera and Imaging Interface Solutions

Camera Interface

Demand for increasingly higher image resolutions is pushing the bandwidth capacity of existing host processor-to-camera sensor interfaces. Common parallel interfaces are difficult to expand, require many interconnects and consume relatively large amounts of power. Emerging serial interfaces address many of the shortcomings of parallel interfaces while introducing their own problems. Incompatible, proprietary interfaces prevent devices from different manufacturers from working together. This can raise system costs and reduce system reliability by requiring “hacks” to force the devices to interoperate. The lack of a clear industry standard can slow innovation and inhibit new product market entry.

CSI-2 provides the mobile industry a standard, robust, scalable, low-power, high-speed, cost-effective interface that supports a wide range of imaging solutions for mobile devices.

The most current revision of the Camera Serial Interface standard is CSI-2 V1.3. The solution consists of a digital controller on the camera device IC (the MIPI CSI-2 Transmitter) and a digital controller on the application or image processor IC (the MIPI CSI-2 Receiver). The controllers connect across a physical layer. There are two physical layer configurations available

- 1 to N MIPI D-PHY lanes plus 1 clock lane. Each lane is a high-speed differential pair. The MIPI D-PHY v1.1 operates at 1.5Gbps. A 4 lane D-PHY layer can transmit 4K video at 30fps.
- 1 to N MIPI C-PHY lanes. Each “lane” is a 3 wire single-ended configuration that encodes video data into 3 bits symbols with the clock embedded. A 3 lane C-PHY v1.0 can transmit 4K video at 60fps.

Display Interface

The MIPI Display Serial Interface is targeted for mobile platforms that integrate a camera sub-system requiring an interface and protocol that allows data to be transmitted from the camera to the host processor. The DSI specification provides device manufacturers a standardized high-performance interface that scales with the increasing frame rates, resolution and pixel depth of the imaging systems.

The most current revision of the Display Serial Interface standard is DSI V1.3. The solution consists of a digital controller on the display device IC (the MIPI DSI Device) and a digital controller on the application or processor IC (the MIPI DSI Host). Like the CSI-2 configuration, the controllers connect across a physical layer comprised of 1 to N MIPI D-PHY lanes plus 1 clock lane. Each lane is a high-speed differential pair. In addition a low-speed I2C serial link is used for camera control. For example a 2 lane D-PHY physical layer would have 8 data pins.

The figures below (for CSI-2) are analogous to figures for DSI-2.

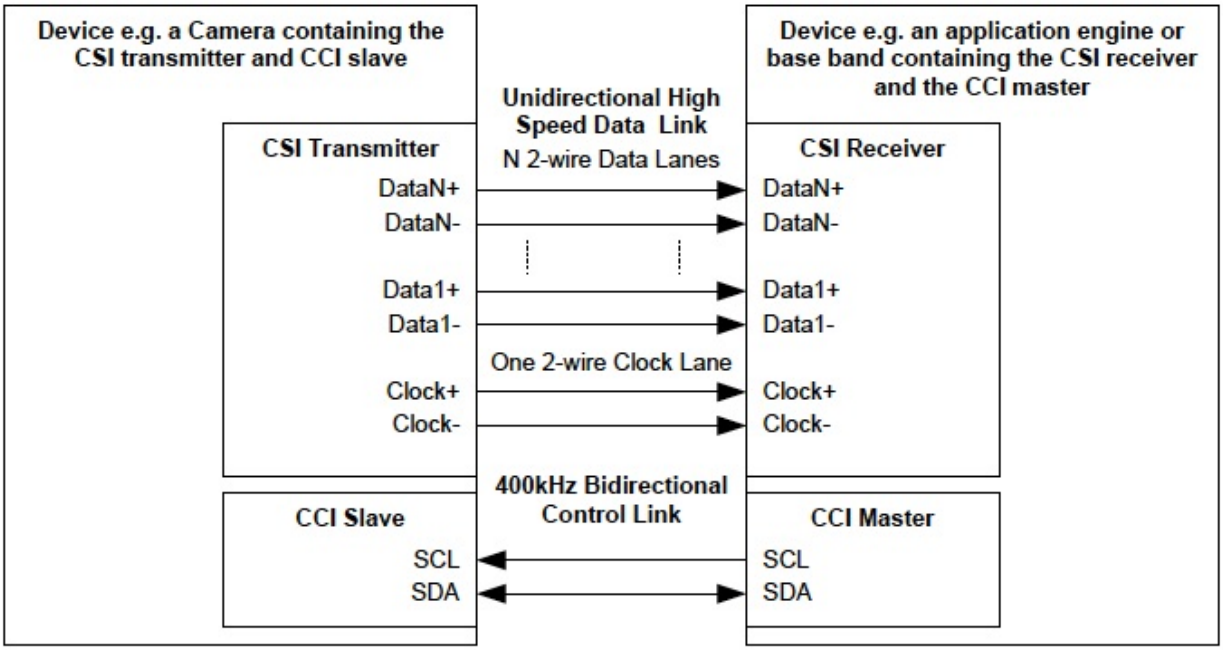

Figure 1a. CSI Interface using a D-PHY signal channel

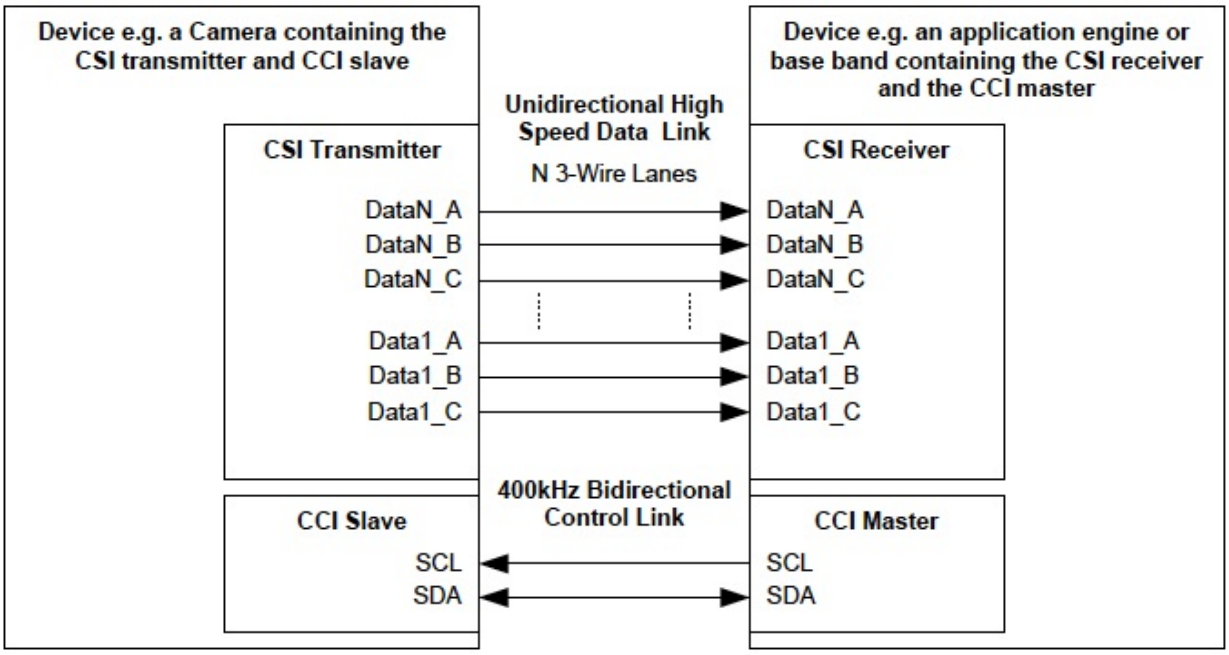

Figure 1b. CSI Interface using C-PHY signal channel

MIPI D-PHY

MIPI D-PHY is the physical interface for CSI-2 and DSI providing 2.5Gbps per lane of bandwidth. The latest board approved specification is D-PHY v2.0 released March 8, 2016. However, this specification is primarily intended to define a solution for a bit-data rate range of 80 to 1500 Mbps per Lane without de-skew calibration, up to 2500 Mbps with de-skew calibration, and up to 4500 Mbps with equalization. When the DUT implementation supports a data rate greater than 1500 Mbps, it shall also support de-skew capability. When a PHY implementation supports a data rate more than 2500 Mbps, it shall also support equalization, and Spread Spectrum Clocking shall be available.

Arasan's MIPI D-PHY Analog Transceiver IP Core is fully compliant to the D-PHY specification version 2.0. It supports the MIPI® Camera Serial Interface (CSI-2) and Display Serial Interface (DSI) protocols. It is a Universal PHY that can be configured as a transmitter, receiver or transceiver. The D-PHY consists of an analog front end to generate and receive the electrical level signals, and a digital (PPI) interface to control the I/O functions.

MIPI C-PHY

The latest board approved specification is C-PHY v1.1 released February 11, 2016. C-PHY provides high throughput performance over bandwidth limited channels for connecting to peripherals, including displays and cameras. The C-PHY is based on 3-Phase symbol encoding technology delivering 2.28 bits per symbol over three-wire trios, targeting 2.5Gsymbols/s. C-PHY has many characteristics in-common with D-PHY. C-PHY was designed to coexist on the same IC pins as D-PHY so that dual-mode devices can be developed.

Performance Comparison

The primary performance metric is bandwidth – megapixel transfer rate for CSI-2 and video display resolution for DSI-2.

	HD	QHD	UHD	8K
Display Size	1920 x 1080	2048x1536	3840x2160	7680x4320
Color bits	24	24	30	30
Gbps @30fps	1.49	2.66	7.47	29.9
Gbps @60fps	2.99	5.32	14.9	note
Gbps @120fps	5.97	10.62	29.9	note
Gbps @240fps	11.94	21.23	note	note

D-PHY v1.1 4 Lanes | C-PHY v1.0 3 Lanes | D-PHY v2.0 4 Lanes

Table 1. Bandwidth Comparison

Key Characteristic of D-PHY

The D-PHY provides a synchronous connection between Master and Slave. A PHY configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the Master and terminating at the Slave. The data signals can either be unidirectional or bi-directional depending on the selected options. For half-duplex operation, the reverse direction bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the Link.

The Link includes a High-Speed signaling mode for fast-data traffic and a Low-Power signaling mode for 180 control purposes. Optionally, a Low-Power Escape mode can be used for low speed asynchronous data communication. High-speed data communication appears in bursts with an arbitrary number of payload data bytes.

The PHY uses two wires per Data Lane plus two wires for the Clock Lane. This gives four wires for the minimum PHY configuration. In High-Speed mode each Lane is terminated on both sides and driven by a low-swing, differential signal. In Low-Power mode all wires are operated single-ended and non-terminated.

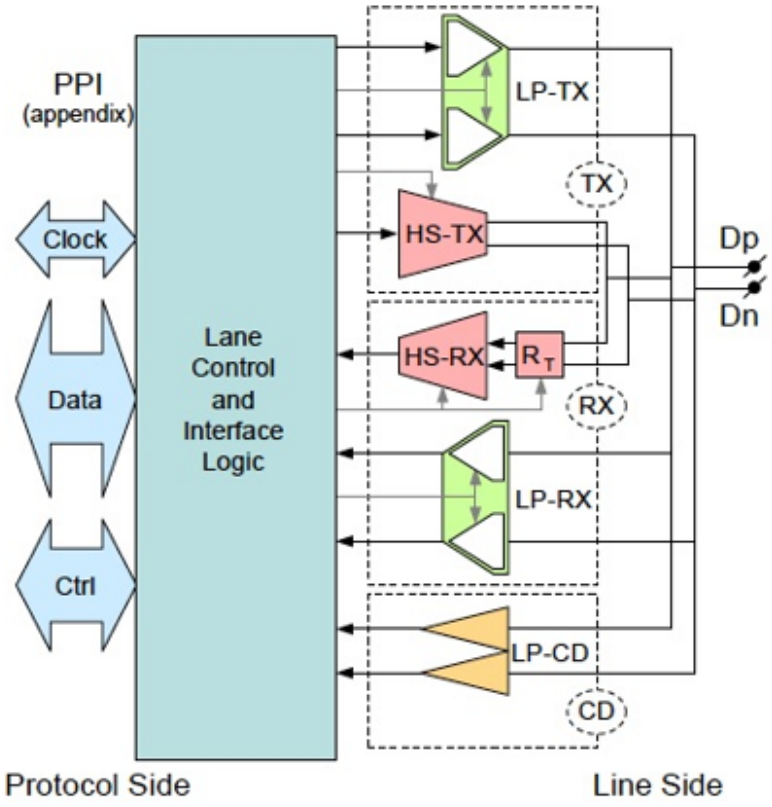

Figure 2. MIPI D-PHY

Key Characteristics of C-PHY

• Uses a group of three conductors rather than conventional pairs. The group of three wires is called a lane, and the individual lines of the lane are called: A, B and C. C-PHY does not have a separate clock lane.

• In a three-wire lane, two of the three wires are driven to opposite levels; the third wire is terminated to a mid-level (at either one end or both ends), and the voltages at which the wires are driven changes at every symbol.

• Multiple bits are encoded into each symbol epoch, the data rate is ~2.28x the symbol rate. There is no additional overhead for line coding, such as 8b10b, which is not needed.

• Clock timing is encoded into each symbol. This is accomplished by requiring that the combination of voltages driven onto the wires must change at every symbol boundary. This simplifies clock recovery.

• The signal is received using a group of three differential receivers.

• The C-PHY interface can co-exist on the same pins/pads as the D-PHY interface signals.

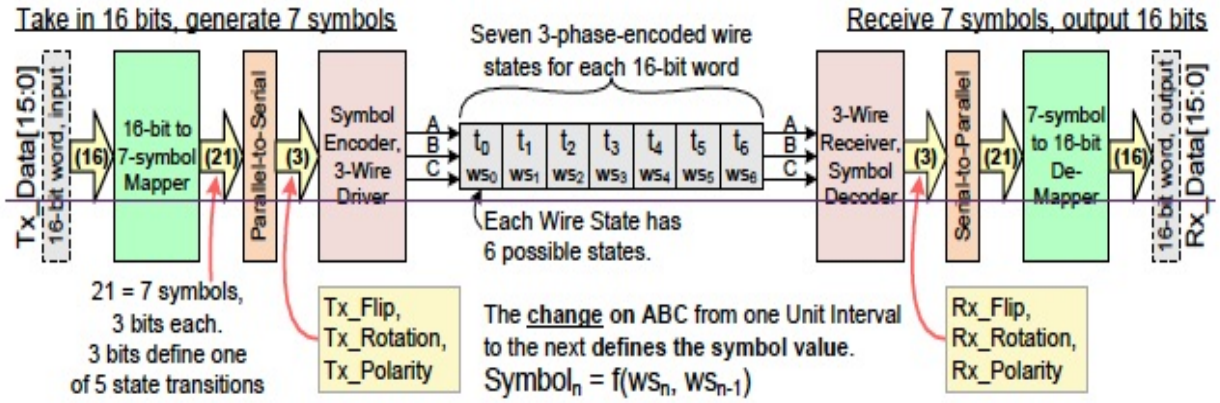

Figure 3. C-PHY Data Flow

The Arasan C-PHY+D-PHY Combination

The ever increasing demand for band width for the high resolution cameras resulted in to search for a simple, cost effective, rate efficient PHY which can support above 2.5Gbps. This search resulted into a new kind of PHY, which even at less channel rate provides very high data rate.

CPHY can achieve a very high data rate of 5.71Gbps per lane compared to the 2.5Gbps of DPHY1.2 or 1.5Gbps of DPHY1.1, still maintain the channel rate at 2.5Gsps which is same as DPHY1.2. CPHY achieves this by using a unique encoding mechanism in which 16 bit of input data is encoded into 7 symbols and each symbol is transmitted over a 3 Phase encoded line.

CPHY reuses the similar Low power signaling same as the DPHY. CPHY is designed such a way that it can co-exist sharing the same lines as DPHY. CPHY/DPHY combo IPs will be compatible to operate on the same channels used by DPHY, which offer a much wider area of application and flexibility. It can work with both old DPHY systems and is compatible with new CPHY. Arasan's ComPHY is a CPHY/DPHY combo universal PHY which can be configured both as Transmitter and Receiver.

Arasan's CPHY-DPHY combination provides a 3 channel C-PHY v1.0 and a four lane D-PHY v1.2 in a single IP core. This allows a seamless implementation allowing interface to D-PHY based sensors or C-PHY based sensors.

Symbol encoding effectively transfers 2.286 bits per symbol compared to 1.0 bits per lane for D-PHY. The first version of C-PHY (v1.0) operates at 2.5GHz, same as the D-PHY V1.2.

A four lane D-PHY V1.2 provides 10Gbps which enables:

- 4K video at 30fps
- 1080p at 120fps

A 3 channel C-PHY provides 17Gbps which enables:

- 4K video at 60fps
- 1080p at 240fps (for cool slow-motion videos)

Benefits of a Combination solution

The primary benefit on the host side is compatibility with any device (C-PHY based or D-PHY based).

PCB routing requirements

- Single ended terminated lines for C-PHY
- Differential small voltage pair for D-PHY

Pin Count is approximately the same

- 3 vs 4 for a one lane implementation (C-PHY vs D-PHY)

9 pins vs 10 for a 4 lane implementation (C-PHY vs D-PHY)

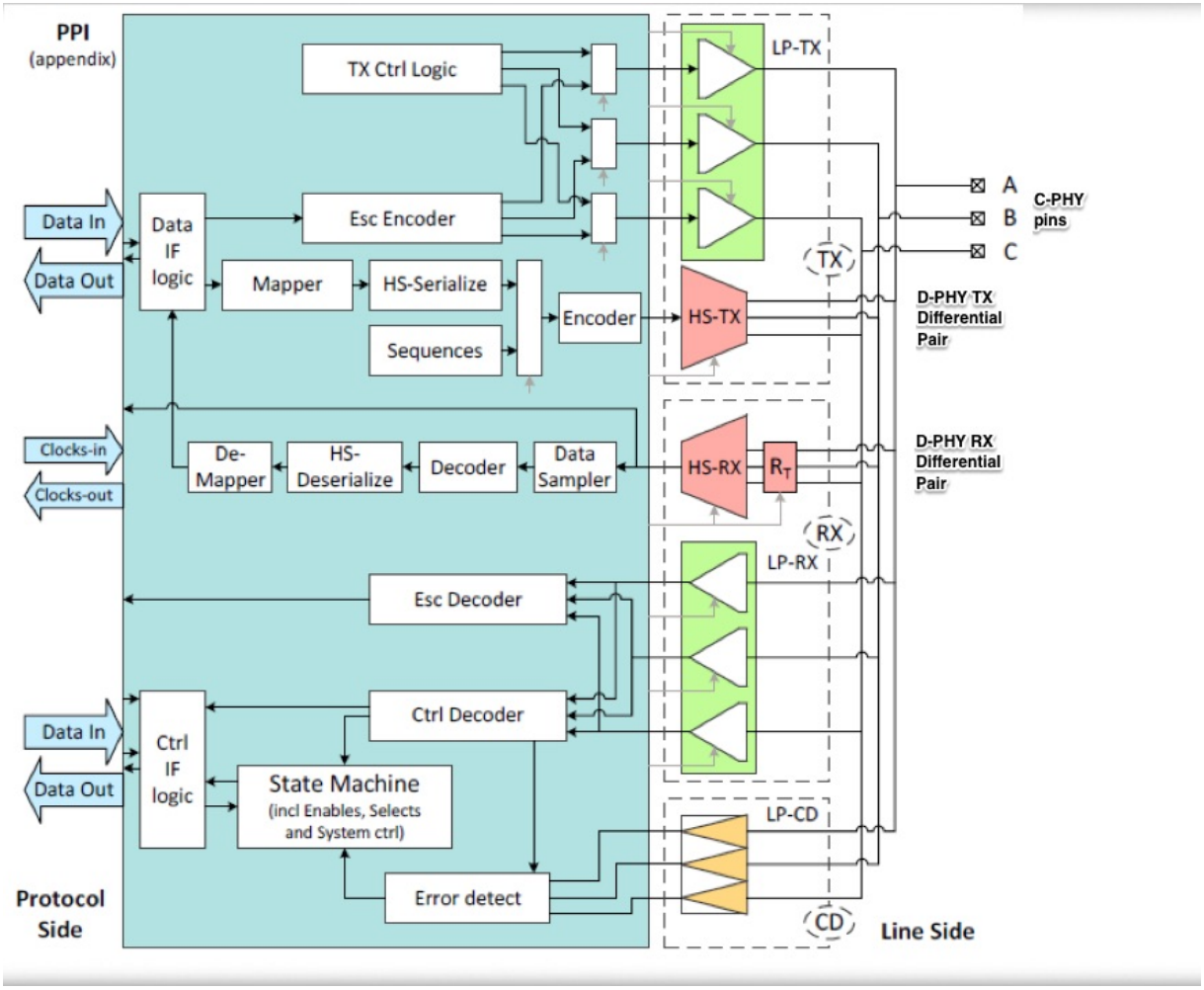

Figure 4. C-PHY / D-PHY Combination I/O

Arasan's MIPI Support

Arasan's Arasan has been a contributing member of MIPI since 2004. Our expertise is deeply embedded in all product offerings. Being intimately involved in developing the standards ensures that Arasan gets a head-start in understanding near-term and future standard roadmaps. This helps the company in planning product updates accordingly and in going to the market with the latest and most innovative products. Customers in turn reap the benefits of being the first mover.

Arasan's strategic partnerships in the IP ecosystem help the company in defining and implementing methods for compliance and interoperability testing. Arasan works with its customers from the onset in defining their MRD and architecting their SoC designs. The company is cognizant of its customers' specific requirements and offers IP customization services to help them achieve product differentiation.

Arasan stands by its solutions with the support network of highly skilled engineers who are directly involved in developing the code and therefore possess an intimate knowledge of the IP standard. Arasan is also one of the very few companies that offer support on customized IP in addition to standard IP.

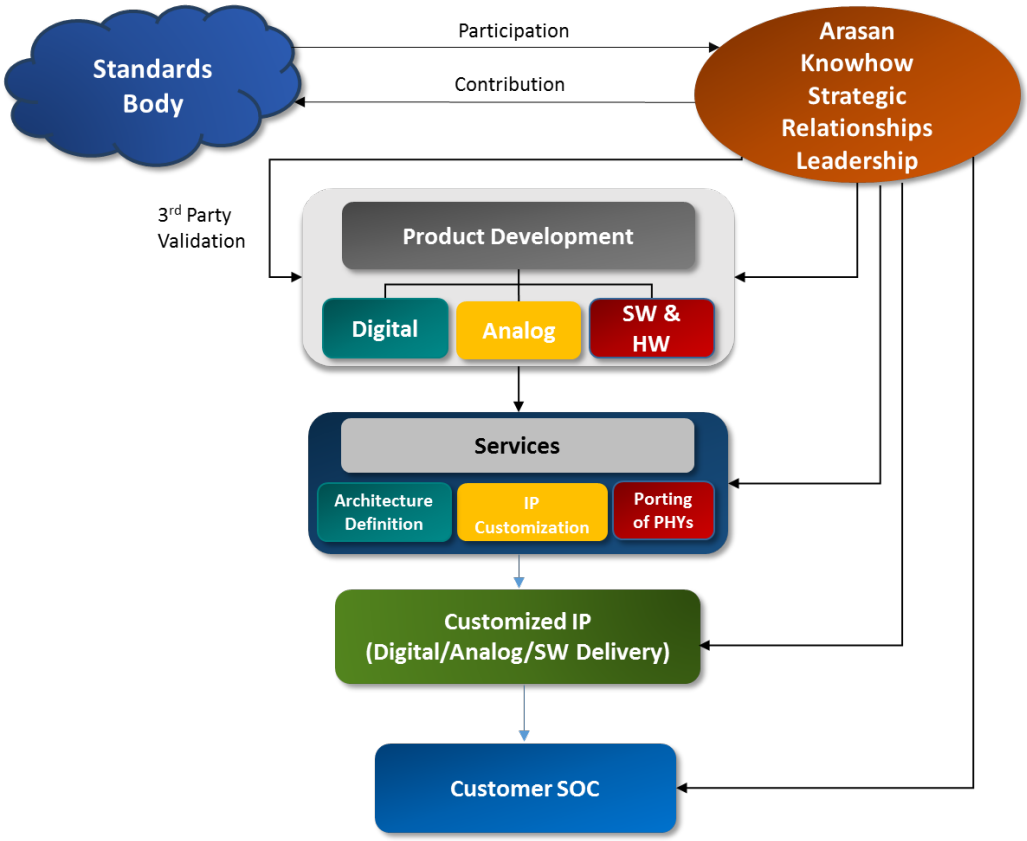

Figure 5. Arasan Standards IP Development