

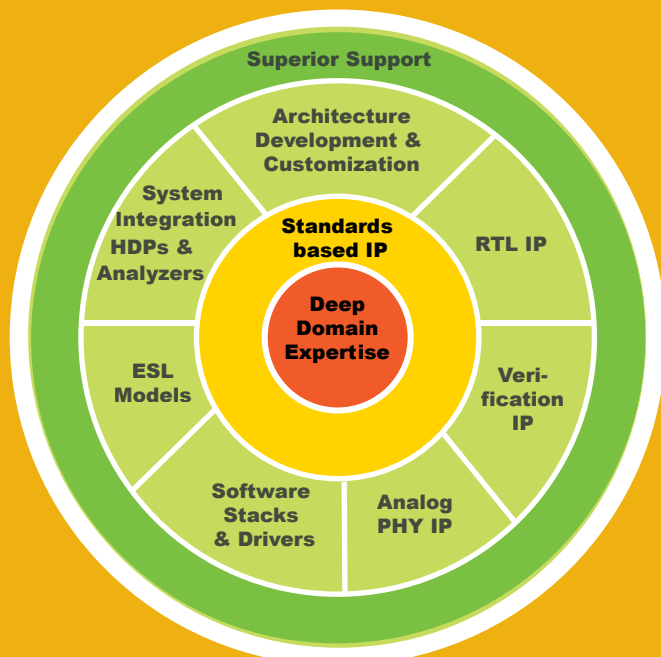
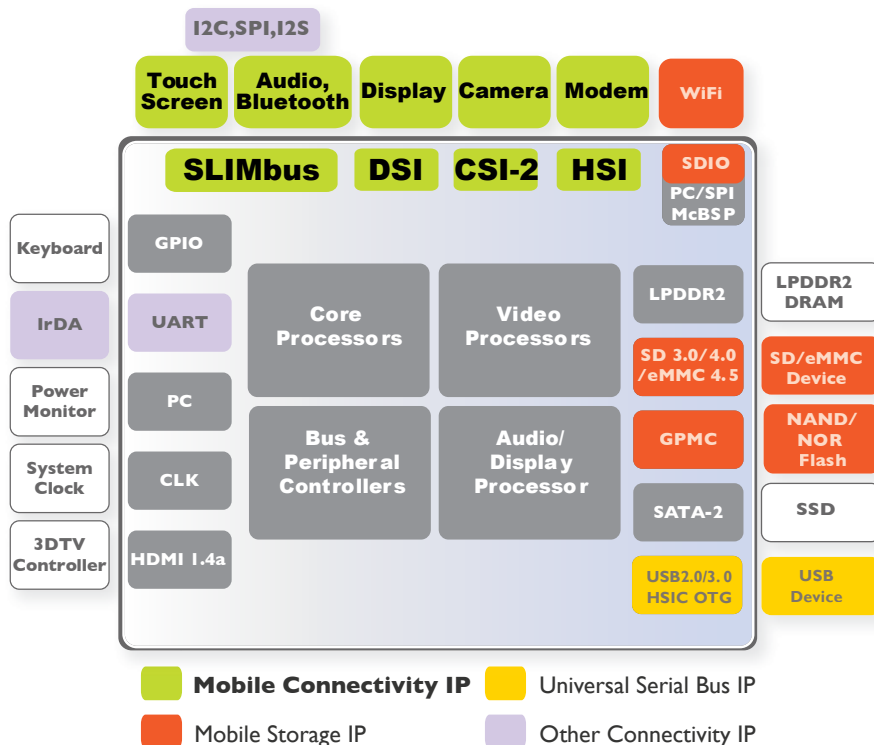


Mobile Connectivity IP

Arasan Chip Systems is a leading provider of Total IP Solutions for mobile storage and connectivity applications. Arasan's comprehensive suite of MIPI® interface IP enables low pin count connectivity between chips and devices on a mobile platform.

Arasan's mobile connectivity IP cores and PHYs implement the most up-to-date versions of CSI-2, DSI, HSI, SLIMbus, Unipro and D-PHY.

For easy integration into your SoC, Arasan's mobile connectivity IP supports many popular on-chip system buses including AXI, AHB, APB, OCP, microcontroller, and custom interfaces.



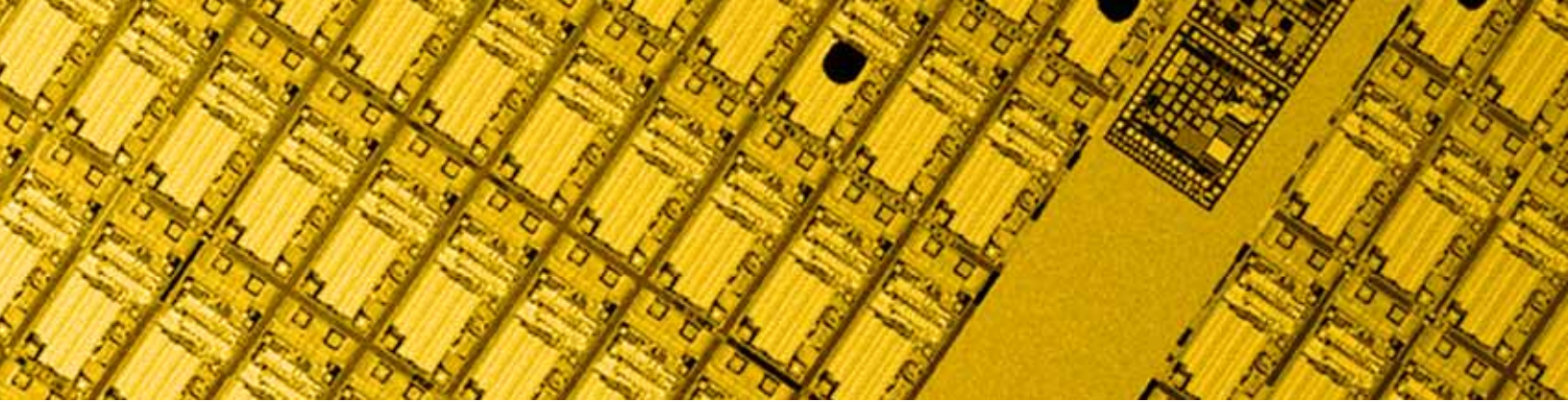
- Market-leading Activities
- Total IP Solution Components
- Continuing Support

Total IP SOLUTIONS

Arasan provides a Total IP Solution which encompasses all aspects of IP development and integration including analog and digital cores, verification IP, software stacks and drivers, ESL models and hardware validation and analysis platform.



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Camera Serial Interface (MIPI CSI-2)

Arasan MIPI CSI-2 version 1.01 compliant Transmitter and Receiver cores comply with the PPI interface of D-PHY 1.0, and support up to 4 lanes with a maximum of 4Gbps throughput. The Receiver, which typically resides in a mobile applications processor, is configured and managed through an AHB interface, while pixel transfers are made through an ISP interface. The Transmitter on a camera module is configured through a microcontroller interface, while pixel transfers are done through a byte aligned image sensor interface. A wide variety of video and display formats and resolutions, with a maximum of 1080p HD, are supported.

Display Serial Interface (MIPI DSI)

Arasan MIPI DSI version 1.02 compliant Host and Device cores also comply with the PPI interface of the D-PHY version 1.0, and support up to 4 lanes. The Host, which typically resides in a mobile applications processor, is configured and managed through an AHB interface, while pixel transfers from an LCD controller are made through either the Display Pixel (DPI) or Display Bus (DBI) Interface. The Device IP resides on a display panel, and has similar interfaces as the Host. A wide variety of video and display formats and resolutions, with a maximum of 1080p HD, are supported.

Serial Low Power Inter-chip Media Bus Interface (MIPI SLIMbus)

Arasan MIPI SLIMbus version 1.01 compliant Host and Device IP cores provide mid to low bandwidth connectivity between applications processors and peripheral components, like audio codecs. Using an active manager, the host manages the SLIMbus sub-system, and allocates TDM bit-serial channels to all devices on the 28.8 MHz bus. Both the host and device contain a framer, interface device and a generic device with up to 8 active port pairs, which in turn interface to the AHB bus, or bridge to I2S, I2C or SPI.

High Speed Synchronous Serial Interface (MIPI HSI)

Arasan MIPI HSI version 1.0 compliant cores enable serial connectivity between two peer components, typically the applications and baseband processors. Maximum transmission rate of 200 Mbps with data split between 1 to 8 logical channels in both transmit and receive directions are supported. 32 bit AHB, AXI or OCP interfaces to the rest of the SoC are available, with Programmed IO used to configure the IP, and scatter-gather DMA used for bulk data transfers to and from system memory.

MIPI D-PHY

Arasan MIPI D-PHY version 1.0 provides the physical layer implementation for CSI-2 and DSI protocols. This IP is delivered in GDS II format, and supports both high speed (80Mbps – 1 Gbps) and low power (10Mbps) differential signaling with link turnaround.

Unified Protocol Interface (MIPI Unipro)

Arasan MIPI Unipro version 1.4 compliant cores provide end to end flow control for two peer devices that communicate over either an M-PHY or D-PHY based serial interface. Data transmission is priority based, and conforms to traffic classes TC0 and TC1. Control, configuration and 32 or 64 bit scatter-gather DMA operations with CPU/memory are supported over the AHB, AXI or OCP buses.

RF Front End Interface (MIPI RFFE)

Arasan MIPI RFFE version 1.0 compliant Master and Slave cores provide the connectivity between RFIC's and RF front end components, like power and low-noise amplifiers and antenna sensors. The Master controller resides in the RFIC, and is programmable through AHB or APB bus. It uses a serial link to connect and program the registers in up to 15 front end Slave devices on the RFFE bus. Both IP's are delivered in RTL form, with a GDS-II option.

DIFFERENTIATION

Arasan provides a Total IP Solution which encompasses all aspects of IP development and integration including analog and digital cores, verification IP, software stacks and drivers, ESL models and hardware validation and analysis platform. In addition, Arasan's product offering is differentiated by:

Deep Domain Expertise

Arasan participates in standards setting bodies for MIPI®, USB, UFS, eMMC/MMC, SD, and ONFI. Arasan uses this domain expertise to assist customers in architecting their solutions and staying current with the rapidly changing standards environment.

Best Quality IP Cores

Silicon-proven cores are IP-XACT compliant, RMM- compliant and have been optimized for power and performance with Atrenta Spyglass. All interfaces are native interfaces, no gaskets, providing for highest throughput.

Early Verification

Arasan's verification IP suite includes bus functional (ESL) models enabling HW/SW integration early in the design process, simplifying and speeding integration.

Customized Solutions

Arasan offers the unique ability to provide customization services such user-side bus modifications, additional FIFOs, and other customer requested features which delivers improved differentiation for the customer's system. Arasan maintains these customizations through its maintenance and upgrade program.

Superior Customer Support

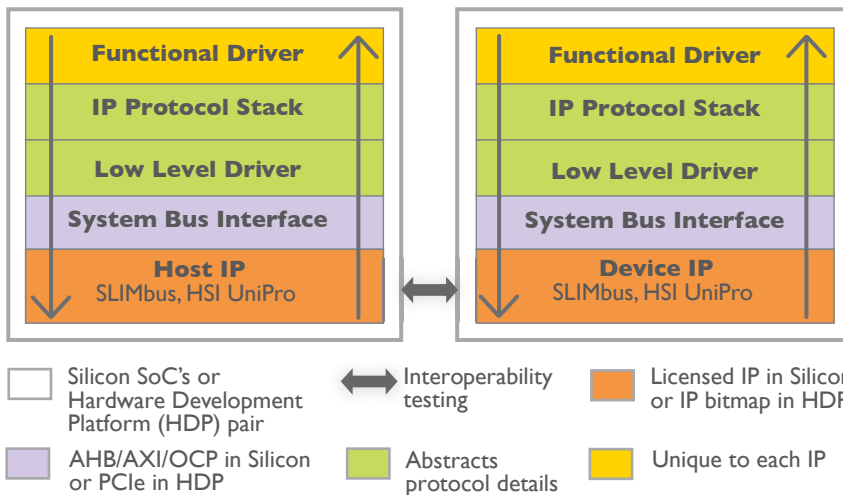
Arasan's development engineering team supports customers directly assuring the highest level of knowledge and fastest problem resolution.



Arasan Total IP Solutions

Arasan's mobile connectivity products serve system architects and SoC design teams who are looking for silicon-proven, validated IP delivered with the ability to integrate and verify digital, analog and software components in the shortest possible time with the lowest risk. These IP solutions have been incorporated into millions of mobile devices including smartphones, tablets, digital cameras, portable game consoles, and many others.

Software Stacks and Hardware Development Platforms



Some protocols, like SLIMbus, HSI and emerging protocols, like CSI-3 and UFS, which are based on Unipro, require entire software stacks for functional driver development. Arasan provides these software stacks as well as porting and customization services. For early software development and to enable interoperability or protocol testing, the IP's and software stacks are mapped into Arasan's Hardware Development Platforms.

About Arasan

Arasan Chip Systems is a leading provider of Total IP Solutions for mobile storage and connectivity applications. Arasan's high-quality, silicon-proven, Total IP Solutions include digital IP cores, analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers, software stacks and drivers and optional customization services for MIPI, USB, SD, SDIO, MMC/eMMC, CF, UFS, xD and many other popular standards.

Arasan's Total IP products serve system architects and chip design teams in mobile, gaming and desktop computing systems that require silicon-proven, validated IP, delivered with the ability to integrate and verify both digital, analog and software components in the shortest possible time with the lowest risk.

Our corporate office is located in San Jose, California. We've been in business for nearly 15 years providing our customers everything they need to deploy our IP in their products. Our goal is to provide our customers with a solution that allows them to quickly integrate our IP while insuring project success.

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