CAN FD Controller IP Core

Arasan CAN FD IP Core Features

- CAN FD IP Core Implements the CAN 2.0A and CAN 2.0B protocol. ISO 11898-1 compliant
- Supports ISO CAN-FD – ISO 11898-1:2015 DIS compliant
- Non-ISO CAN FD - Compliant to Bosch Spec.
- Independent System Clock(SYSCLK) and CAN Bus Clock(CANCLK)
  - SYSCLK is CPU interface Bus Clock, - AHB Clock in case of ARM
  - CANCLK can either be independent or tied to SYSCLK
- Flexible shared buffering scheme that implements optimal buffer size for Transmit and Receive messages
  - Total buffer size is parameterized - synthesis time option
  - Buffer can be implemented as a single port SRAM or flops
  - Transmit buffer, receiver buffer and high-priority transmit buffer
  - CPU configurable depths for transmit, receive and high-priority transmit buffers
- Parameterized number of Acceptance Filters - 1-16
- AHB-Lite Slave Interface for connecting to CPU
  - Optional APB Interface
  - Supports 32-bit interface
- Programmable Baud Rate Prescalar (BRP)
  - Generate Time Quantum Clock from CANCLK
  - 8-bit BRP register to have div-by-2 up to div-by-255

Arasan CAN FD IP Core Benefits

- Fully compliant to ISO 11898-1:2015 DIS
- Small footprint
- Code validated with Spyglass
- Functionality ensured with comprehensive verification with 3rd party VIPs
- Functionality proved in FPGA
- Direct support from Arasan CAN IP Core Designers

Overview

The Controller Area Network – Flexible Data (CAN-FD) controller IP implements the CAN 2.0A, CAN 2.0B as well as newer high performance CAN-FD protocols. It is compliant to both Non-ISO CAN FD from Bosch as wells ISO 11898-1:2015 DIS

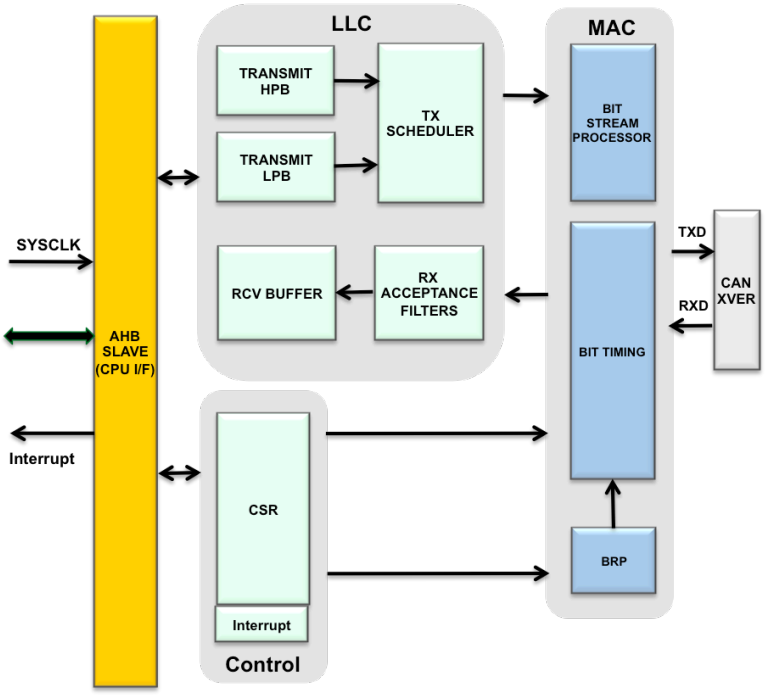
It can be integrated into devices that require CAN connectivity commonly used in automotive and industrial applications.

The Controller

The Controller Area Network – Flexible Data (CAN-FD) controller IP.

The Transceiver

The CAN FD Transceiver IP core is also available. Compliant to ISO 11898-2 and ISO 11898-5 specifications.



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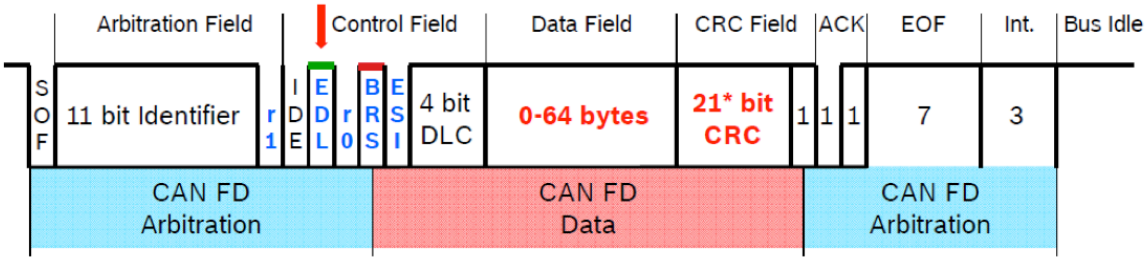
The Bus and Packet etc.

The CAN FD Controller IP Core.



* 17 bit CRC for data fields with up to 16 bytes

- CAN FD Arbitration Phase
  - length: 30 bit times*
  - data rate: max. 1 MBit/s
- CAN FD Data Phase
  - length: 86 bit times* (8 data bytes)
  - data rate: > 1 MBit/s
- Remote Frames always in CAN Format
  - RTR bit replaced by reserved bit r1
  - r1 takes part in CAN arbitration
  - reserved for protocol expansion

* bit stuffing not considered

EDL – Extended Data Length
Substitutes first reserved bit in standard frames
EDL = recessive indicates CAN FD frame format
(new DLC-coding and CRC)
EDL = dominant indicates standard CAN frame format

r1, r0 – reserved bits
Transmitted dominant, reserved for future protocol variants

BRS – Bit Rate Switch
BRS = recessive: switch to alternate bit rate
BRS = dominant: do not switch bit rate

ESI – Error State Indicator
ESI = recessive: transmitting node is error passive
ESI = dominant: transmitting node is error active

DELIVERABLES

CAN FD IP Core
- RMM Compliant Verilog RTL Source Code
- Comprehensive Verilog Test Environment & Compliance Suite
- UVM based Test Environment
- Sample Firmware & HDK

CAN FD Transceiver IP Core
- GDS II of the CAN FD Transceiver
- BIST Guidelines
- User Manual & IP Integration Guide

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