Datasheet

MIPI D-PHY v1.2 Physical Interface

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1 Introduction

1.1 About MIPI CSI and DSI

The MIPI®Alliance the Camera Serial Interface (CSI-2) defines protocols between a Camera device (transmit) and the host processor (receive) using a D-PHY physical interface. D-PHY v1.2 is compatible with CSI-2 v1.3 and earlier versions back to CSI-2 v1.1.

The MIPI Display Serial Interface (DSI) specification defines protocols between a host processor (transmit) and display modules (receive) using a D-PHY physical interface. The DSI specification builds on existing specifications by adopting pixel formats and command set defined in MIPI Alliance Specifications for Display Pixel Interface 2 (DPI-2) and Display Command Set (DCS).

D-PHY v1.2 is compatible with DSI v1.3 and DSI-2 v1.0 and prior versions back to DSI v1.1

Demand for increasingly higher image resolutions is pushing the bandwidth capacity of existing host processor-to-camera sensor interfaces. Common parallel interfaces are difficult to expand, require many interconnects and consume relatively large amounts of power. Emerging serial interfaces address many of the shortcomings of parallel interfaces while introducing their own problems. Incompatible, proprietary interfaces prevent devices from different manufacturers from working together. This can raise system costs and reduce system reliability by requiring “hacks” to force the devices to interoperate. The lack of a clear industry standard can slow innovation and inhibit new product market entry.

1.2 Arasan’s Contribution to MIPI

Arasan has been a member of MIPI for over ten years. We are active participants in a number of working groups. We work closely with other member customers to ensure compliant implementation of standards based IP.

1.3 Arasan’s Total IP Solution

Arasan provides a Total IP Solution, which encompasses all aspects of IP development and integration, including analog and digital IP cores, verification IP, software stacks & drivers, and hardware validation platforms. Benefits of Total IP Solution:

- Seamless integration from PHY to Software
- Assured compliance across all components
- Single point of support
- Easiest acquisition process (one licensing source)
- Lowest overall cost including cost of integration
- Lowest risk for fast time to market

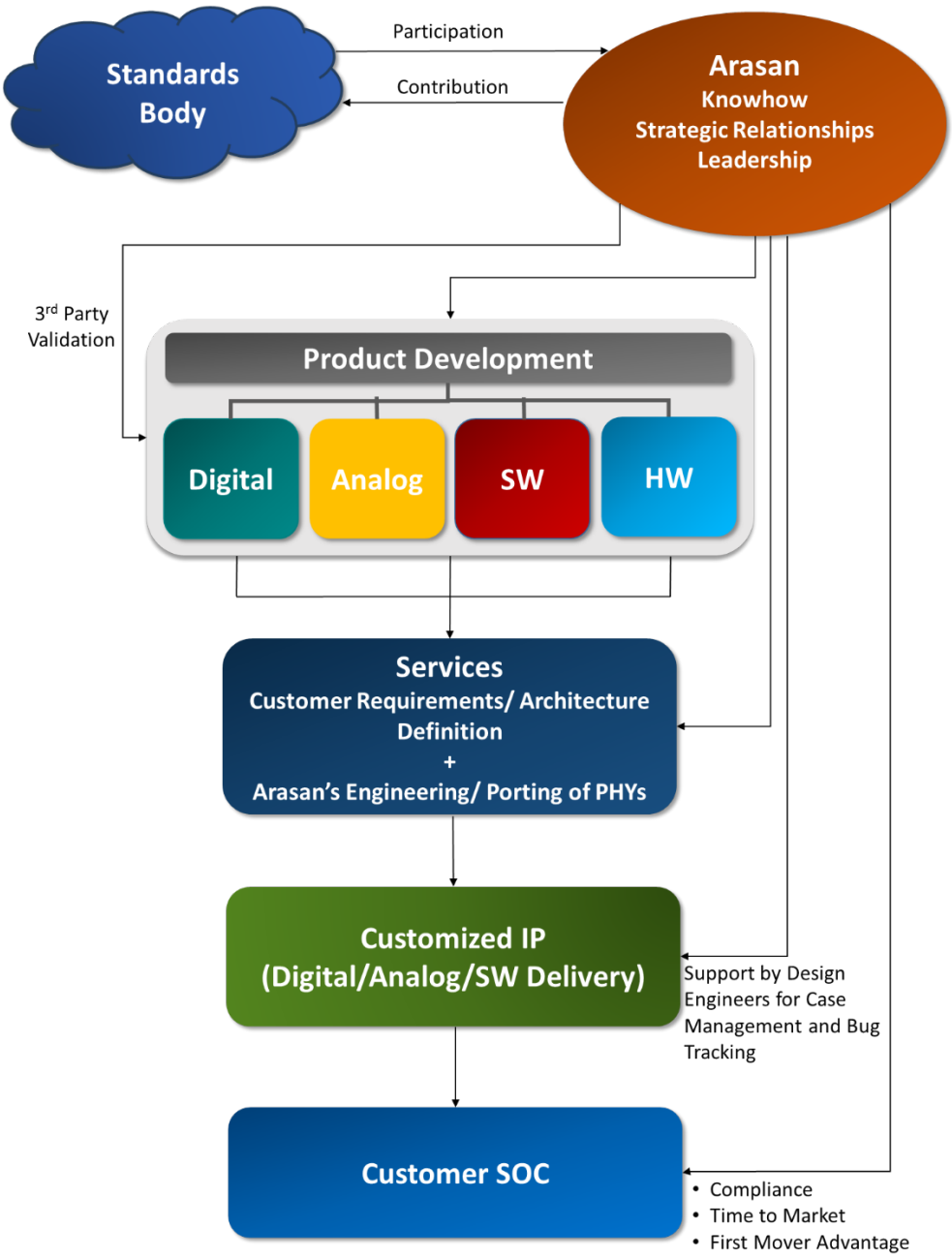

Figure 1: Arasan's Total IP Solution

2 D-PHY v1.2 Physical Interface IP

2.1 Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI®) Alliance was created to define and promote open standards for interfaces to mobile application processors. D-PHY is the physical layer specified for several of the key protocols within the MIPI® family of specifications.

The Arasan D-PHY IP core is fully compliant to the D-PHY specification version 1.2. It supports the MIPI® Camera Serial Interface (CSI-2) and Display Serial Interface (DSI) protocols. It is a universal PHY that can be configured as a transmitter, receiver or transceiver. The D-PHY consists of an analog front end to generate and receive the electrical level signals, and a digital back end to control the I/O functions.

The Arasan D-PHY provides a point to point connection between master and slave or host and device that comply with a relevant MIPI® standard. A typical configuration consists of a clock lane and 1-4 data lanes. The master/host is primarily the source of data and the slave/device is usually the sink of data. The D-PHY lanes can be configured for unidirectional or bidirectional lane operation, originating at the master and terminating at the slave. It can be configured to operate as a master or as a slave. The D-PHY link supports a high speed (HS) mode for fast data traffic and a low power (LP) mode for control transactions. In HS mode, the low swing differential signal is able to support data transfers from 80 Mbps to 1500 Mbps per lane without deskew calibration and up to 2500 Mbps with deskew calibration. In LP mode all wires operate as a single ended line capable of supporting 10 Mbps asynchronous data communications.

The Arasan D-PHY IP core implements the PPI interface recommended by the MIPI® working groups to easily interface to the required protocols.

2.2 Features

- Compliant to MIPI Alliance Standard for D-PHY specification Version 1.2. Supports:
- Synchronous transfer at high speed mode with a bit rate of 80-2500 Mb/s
- Asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low Power [LP] data
- One byte buffer housed inside the core for both data-out and data-in paths.
- One clock lane and up to four data lanes
- Error detection mechanism for sequence errors and contentions
- Transfer of data in high speed mode
- Ultra low power mode, high speed mode and escape mode.
- Contention detection and turnarounds

- Clock divider unit to generate clock for parallel data reception and transmission from and to the PPI unit.
- Activation and disconnection of high speed terminators for reception and transmission.
- Standard PHY transceiver compliant to MIPI Specification
- Standard PPI interface compliant to MIPI Specification.
- Clock lane unidirectional communication
- On-chip clock generation configurable for either transmitter or a receiver
- Testability for Tx, Rx and PLL
- Configurability of PHY as a master or slave
- Core structured to increase the number of data lanes
- High speed mode in Forward communication

2.3 Architecture

2.3.1 D-PHY Based Interconnect Architecture

Physical connectivity between a master and slave component requires a clock lane and, depending on bandwidth needs, one to four data lanes. To support this, a D-PHY has a Clock Lane Module, and one to four Data Lane Modules. Each of these D-PHY Lane Modules communicates via a differential signal pair to a complementary part on the other side of the Lane Interconnect.

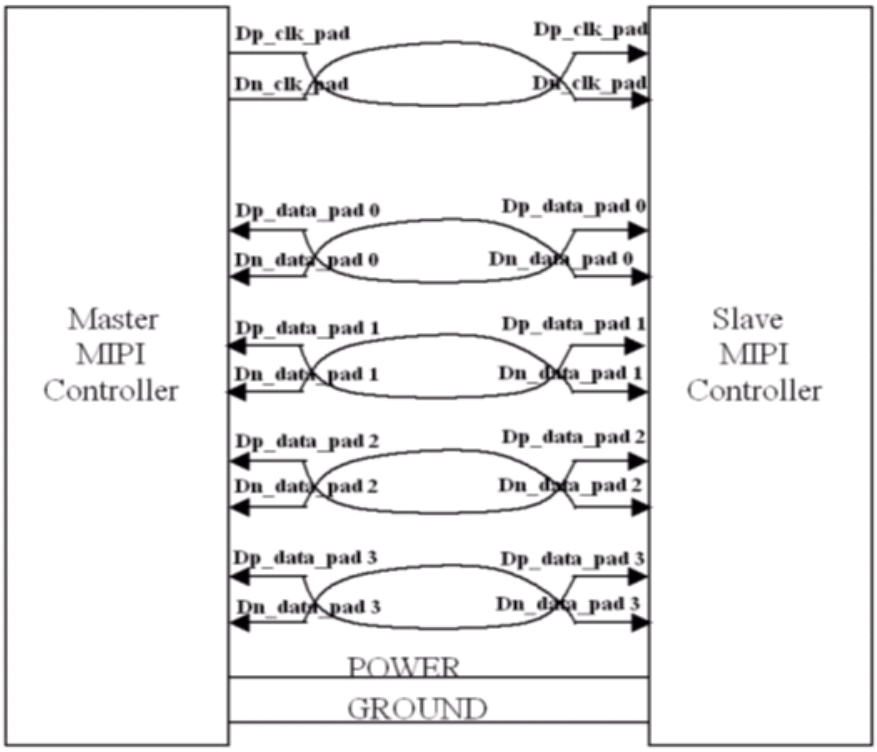

Figure 2: MIPI Link Diagram for Four Data Lanes

2.3.2 D-PHY Lane Architecture

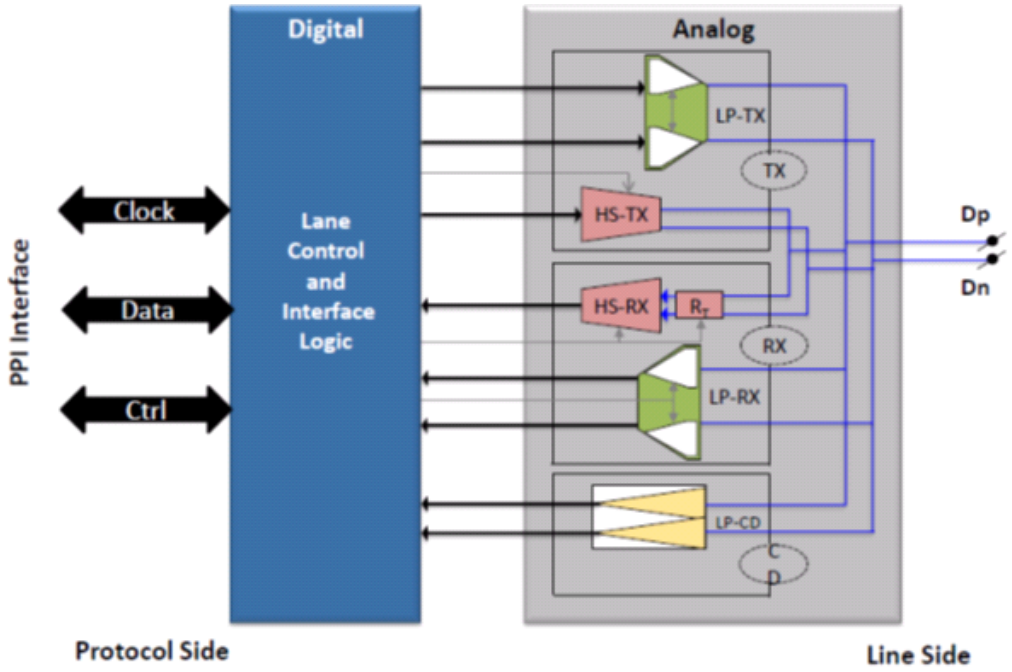

Figure 3: D-PHY Lane Architecture

2.3.2.1 Lane

Each Lane Module has a control and interface logic unit and a transceiver portion to handle differential High-Speed functions utilizing both interconnect wires simultaneously, single-ended Low-Power functions operating on each of the interconnect wires individually and a low power contention detector. The I/O functions are controlled by a Lane Control and Interface Logic block.

2.3.2.2 Signaling

High-Speed signals have a low voltage swing of 200 mV, while Low-Power signals have a large swing of 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for control and can have data transfer support.

2.3.2.3 Link

Each link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. This main direction of communication is denoted as the Forward direction. Communication in the opposite direction is called Reverse traffic. Only bi-directional Data Lanes support both forward and reverse communications.

2.3.2.4 Lane Control and Interface Logic

It sends and detects start of packet signalling and end of packet signalling on the data lanes. It has a serializer and de-serializer unit to dialog with the PPI / PHY adapter unit. Also it has clock divider unit to source and receive data during parallel data transfers from and to the PPI.

2.4 Arasan D-PHY Architecture

The transceiver pins of the Arasan D-PHY are compliant to MIPI's transceivers. The lane control and interface logic unit operates with the clock provided by PPI unit during high speed as well as in low power modes of operation in master mode whereas, a separate low power clock is used in slave mode for low power operations and the received high speed clock is used for high speed data transfers.

In Arasan D-PHY digital IP, both Master and slave modes have state machines to generate sequences for switching to high speed, control mode and ultra low power modes. They have deserializer/serializer unit to convert parallel to serial data and vice-versa.

Slave device has sequence observer state machines to know the modes of operation of the lanes. They have sequence error detectors also.

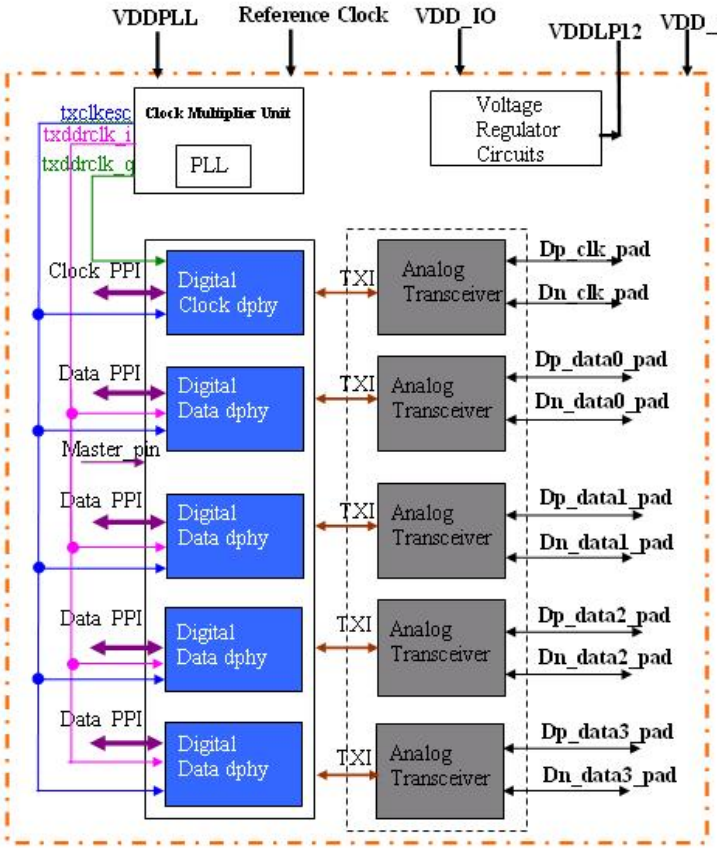

Figure 4: Analog and Digital D-PHY Block Diagram

2.5 D-PHY Pad Table

2.5.1 Functional Description of D-PHY Pads for Clock Lane

Table 1: Functional Description of D-PHY Pads for Clock Lanes

Pin	Direction	Description
dpck	Bidirectional	Positive polarity of low voltage differential clock signal for transmitter and receiver
dnck	Bidirectional	Negative polarity of low voltage differential clock signal for transmitter and receiver

2.5.2 Functional Description of D-PHY Pads for First Data Lane

Table 2: Functional Description of D-PHY Pads for First Data Lane

Pin	Direction	Description
dp0	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn0	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

2.5.3 Functional Description of D-PHY Pads for Second Data Lane

Table 3: Functional Description of D-PHY Pads for Second Data Lane

Pin	Direction	Description
dp1	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn1	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

2.5.4 Functional Description of D-PHY Pads for Third Data Lane

Table 4: Functional Description of D-PHY Pads for Third Data Lane

Pin	Direction	Description
dp2	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn2	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

2.5.5 Functional Description of D-PHY Pads for Fourth Data Lane

Table 5: Functional Description of D-PHY Pads for Fourth Data Lane

Pin	Direction	Description
dp3	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn3	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

2.5.6 Power Pads

Table 6: Power Pads

Pin	Type	Direction	Description
VDD_clk	Power	InOut	Power pad for Clock lane
VSS_clk	Power	InOut	Ground pad for Clock lane
VDD_d0d1	Power	InOut	Power pad for Data lane 0 and Data lane1
VSS_d0d1	Power	InOut	Ground pad for Data lane 0 and Data lane1
VDD_d2d3	Power	InOut	Power pad for Data lane 2 and Data lane 3
VSS_d2d3	Power	InOut	Ground pad for Data lane 2 and Data lane 3
VDDD	Power	InOut	Power pad for DFE
VSSD	Power	InOut	Ground pad for DFE
VDDLP12	Power	InOut	Power pad for Low power blocks

2.5.7 Functional Description of Trim Bits

Table 7: Ports for Trim_Bits

Pin	Direction	Description
trim_0[31:0]	Input	Trim bits for DPHY
trim_1[31:0]	Input	Trim bits for DPHY
trim_2[31:0]	Input	Trim bits for DPHY
trim_3[31:0]	Input	Trim bits for DPHY

2.5.8 Functional Description of Clock and Reset Unit Input

Table 8: Functional Description of Clock and Reset unit Input signals for clock and data PPI

Pin	Direction	Description
TxClkEsc	Input	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL
enable [Reset]	Input	Active Low system reset to the module.

2.5.9 Functional Description of Data PPI Signals Common to all Data Lanes

Table 9: Functional Description of data PPI signals that are common to all Data Lanes

Pin	Direction	Description
dln_bd_ForceRxmode	Input	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.
dln_ForceTxStopmode[3:0]	Input	Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines.

2.5.10 Functional Description of Clock PPI's Escape Mode Signals

Table 10: Functional Description of Clock PPI's High Speed Interface Signals

Pin	Direction	Description
cln_TxRequestHS	Input	High-Speed Transmit Request and Data Valid for clock lane. For clock Lanes, this active high signal causes the lane module to begin transmitting a high-speed clock.
cln_RxActiveHS	Output	Receiver Clock Active. This asynchronous, active high signal indicates that a clock Lane is receiving a DDR clock signal
TxByteClkHS	Output	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. It is recommended that all transmitting Data Lane Modules share one transmitter's byte clock signal. The frequency of byte clock is exactly 1/8 the High-Speed bit rate This is the txbyteclkhs to which all PPI interface is synchronous for transmitter.

RxByteClkHS	Output	High-Speed Receive Byte Clock. This is used to synchronize signals in the High-Speed receive clock domain. The rxbyteclkhs is generated by dividing the received High-Speed DDR clock This is the byte clock to which all PPI interface is synchronous for receiver.
RxDDRClkHS_0	Output	High speed DDR clock used by the receiver.
cln_TxUlpsExit	Input	Transmit ULP Exit Sequence for clock lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when tx_ulpsactivenot_clk_n becomes deasserted. txulpsexit_clk is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State
cln_TxUlpsClk	Input	To force the clock lane to transmit ULPS sequences in the clock line.
cln_RxUlpsClkNot	Output	Receive Ultra Low-Power mode on Clock Lane. This active low signal is asserted to indicate that the Clock Lane module has entered the Ultra Low-Power mode. The Lane module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect
cln_tx_UlpsActive Not	Output	ULP State (not) Active for clock lane. This active low signal is asserted to indicate that the Lane is in ULP state.
cln_rx_UlpsActiveN ot	Output	ULP State (not) Active for clock lane. This active low signal is asserted to indicate that the Lane is in ULP state

2.5.11 Functional Description of Clock PPI's Control Signals

Table 11: Functional Description of Clock PPI's Control Signals

Pin	Direction	Description
cln_Rxstopstate	Output	Lane is in Stop state for clock lane. This active high signal indicates that the lane module is currently in Stop state. This is valid for both receivers and transmitters. Note that this signal is asynchronous to any clock in the PPI interface

2.5.12 Functional Description of Clock PPI's High Speed Interface Signals

Table 12: Functional Description of Data PPI's High Speed Interface signals

Pin	Direction	Description
dln_TxDataHS[31:0]	Input	High-Speed Transmit Data for data lane. High-speed data to be transmitted. Data is captured on rising edges of transmitted byte clock.
dln_TxRequestHS [3:0]	Input	High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on txrequesths causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on txrequesths causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on txdatahs_0 to be transmitted. The lane module accepts the data when both txrequesths and txreadyhs are active on the same rising txbyteclkhs clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, txdatahs remains high until the data has been accepted, as indicated by txreadyhs. txdatahs is only asserted while txrequestesc_0 is low
dln_TxReadyHS [3:0]	Output	High-Speed Transmit Ready for data lane. This active high signal indicates that txdatahs_0 is accepted by the lane module to be serially transmitted. txreadyhs_0 is valid on rising edges of transmitted byte clock.
dln_RxDataHS[31:0]	Output	High-Speed Receive Data for data lane. The signal connected to rxdatahs_0 was received first. Data is transferred on rising edges of receiver byte clock.
dln_RxValidHS[3:0]	Output	High-Speed Receive Data Valid for data lane.
dln_RxActiveHS [3:0]	Output	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.
dln_RxSyncHS[3:0]	Output	Receiver Synchronization Observed for data lane. This active high signal indicates that the Lane module has seen an appropriate synchronization event. In a typical high-speed transmission, rxsynchs_0 is high for one cycle of received byte clock at the beginning of a high-speed transmission when rxactivehs_0 is first asserted, and again for one cycle of received byte clock at the end of a high-speed transmission, just before rxvalidhs_0 returns low.

2.5.13 Functional Description of Data PPI's Escape Mode Signals

Table 13: Functional Description of Data PPI's Escape mode Signals

Pin	Direction	Description
dln_TxRequestEsc [3:0]	Input	Escape mode Transmit Request for data lane . txrequestesc_0 is only asserted by the protocol while txrequesths_0 is low.
dln_TxUlpsExit[3:0]	Input	Transmit ULP Exit Sequence for data lane 0. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes deasserted. txulpsexit_0 is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State.
dln_TxUlpsEsc[3:0]	Input	Escape mode Transmit Ultra Low Power for data lane 0. This active high signal is asserted with txrequestesc to cause the lane module to enter the ultra-low power mode. The lane module remains in this mode until txrequestesc_0 is deasserted. txlpdtesc_0 and all bits of txtriggeresc are low when txulpsesc_0 is asserted.
dln_bd_TxLpdtEsc	Input	This signal is used to request a low power data transmission entry in the reverse direction.
dln_bd_TxTriggerEsc[3:0]	Input	A 4 bit signal that triggers a trigger sequence in the ESC mode in the reverse direction.
dln_bd_TxDataEsc [7:0]	Input	In data mode, the 8-bit data to be transmitted in the reverse direction.
dln_bd_TxValidEsc	Input	A valid signal which qualifies for the data lines.
dln_bd_TurnDisable	Input	To avoid the turn-around request during the lock up situation.
dln_bd_Direction	OutPut	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input).
dln_bd_TurnRequest	Input	This signal is used to request a turn-around operation for a bidirectional lane.
dln_rx_RxClkEsc [3:0]	Output	Escape mode Receive Clock for data lane 0. This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic.

Pin	Direction	Description
dln_rx_RxUlpsEsc[3:0]	Output	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra-low power mode. The lane module remains in this mode with rxulpsesc asserted until a Stop state is detected on the lane interconnect.
dln_rx_UlpsActiveNot[3:0]	Output	ULPS signal received on the receiver in the bi-directional lane
dln_bd_TxReadyEsc	Output	Ready signal for the transmit data lines in reverse direction.
dln_rx_RxDataEsc[7:0]	Output	The low power mode data in the Escape mode.
dln_rx_RxValidEsc	Output	The ESC mode valid data.
dln_rx_RxTriggerEsc[3:0]	Output	The Trigger mode receiver signal.
dln_rx_RxLpdtEsc	Output	The low power data transfer for the first lane
dln_rx_ErrEsc	Output	Error on the Escape sequence during receiver
dln_rx_ErrSyncEsc	Output	Error in sync esc in the receiver mode.

2.5.14 Functional Description of Data PPI's Control Signals

Table 14: Functional Description of Data PPI's Control Signals

Pin	Direction	Description
dln_RxStopState[3:0]	Output	Lane is in Stop state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.
dln_tx_UlpsActiveNot[3:0]	Output	ULP State (not) Active for data lane. This active low signal is asserted to indicate that the Lane is in ULP state.
dln_ErrorSotHS[3:0]	Output	Start-of-Transmission (SoT) Error for data lane. If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of receiver's byte clock. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
dln_ErrorSotSyncHS[3:0]	Output	Start-of-Transmission Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted

Pin	Direction	Description
		in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of receiver's byte clock.
dln_ErrContention LP0	Output	The contention error signal on LP0 line.
dln_ErrContention LP1	Output	The contention error signal on LP1 line.
dln_rx_ErrControl [3:0]	Output	Error control in lane 0 during receiver

2.5.15 Functional Description of Side Band Signals

Table 15: Functional Description of Side Band Signals

Pin	Direction	Description
dln_def_dir	Input	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.
dln_dpdnswap[3:0]	Input	Enable dp dn swap on data lanes 0 to 3 in HS Tx mode.
cln_pll_locked	Output	Pll locked signal from the Dphy

2.5.16 Functional Description of DFT Signals

Table 16: Functional Description of DFT Signals

Pin	Direction	Description
SCAN_EN	Input	Scan mode Enable.
SCAN_CLK	Input	Scan clock
SA_SCAN	Input	Stuck-At scan mode.
SCAN_IN	Input	Scan input for At-speed scan.
SCAN_OUT	Output	Scan output for At-speed scan.
DFT_sdi_1 to 6	Input	Scan input for At-speed scan.
DFT_sdo_1 to 6	Output	Scan output for At-speed scan.

2.5.17 D-PHY UI Parameter Count Signals

Table 17: D-PHY UI Parameter Count Signals

Pin	Type	Direction	Description
dln_cnt_hs_prep[7:0]	Register	Input	The period for which HS prepare time should be accommodated for data lane[40ns]
dln_cnt_hs_zero[7:0]	Register	Input	count [260ns] for Tclock count.
dln_cnt_hs_trail[7:0]	Register	Input	The period for which HS trailing should be driven for data lane[60ns].
dln_cnt_hs_exit[7:0]	Register	Input	The period for which HS exit state should be maintained for data lane[110ns].
dln_rx_cnt[7:0]	Register	Input	Counter that controls the assertion of enable on the DPHY for data lane
dln_sync_cnt[7:0]	Register	Input	A timeout value used for sync error detector logic for data lane.
dln_cnt_lpx[7:0]	Register	Input	Wait time in byte data for the LPX for data lane.
cln_cnt_hs_trail[7:0]	Register	Input	Wait time in byte clock for the trailing bits for clock lane[60ns].
cln_cnt_hs_exit[7:0]	Register	Input	wait time in byte clock for the exit state for clock lane[110ns]
cln_cnt_lpx[7:0]	Register	Input	wait time in byte clock for the LPX for clock lane.
cln_cnt_prep[7:0]	Register	Input	wait time in byte clock for the prepare time for clock lane[40ns]
cln_cnt_zero[7:0]	Register	Input	wait time in byte clock for the zero state for clock lane[260ns].
cln_cnt_pll[15:0]	Register	Input	The count value which is used for the PLL lock time.
dln_cnt_lpx[7:0]	Register	Input	The period for which the LP state should be driven.

2.5.18 A-BIST Related Signals

Table 18: A-BIST Pins

Pin	Direction	Description
dln_loop_back	Input	Enable A-BIST (loopback BIST)
bist_seed[7:0]	Input	BIST PRBS intiation seed
bist_force_error	Input	Signal is used to introduce errors in the BIST run.

Pin	Direction	Description
bist_en_esc_lp, bist_en_esc_hs	Input	Bist mode selection pins 00-> Reserved 01-> HS Mode 10-> LP Mode 11-> RxClkEsc Generation
bist_err_rx_hs	Output	Error in HS reception
bist_err_rx_hs_sync	Output	Error in RX HS sync
bist_err_rx_esc	Output	Error in LP reception
bist_err_rx_esc_ sync	Output	Error in LP rx sync
bist_done	Output	End of BIST comparison

2.6 Hard Macro Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User-guide and integration guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models

3 Services & Support

3.1 Global Support

Arasan Chip Systems provide global support to its IP customers. The technical support is not geographically bound to any specific site or location, and therefore our customers can easily get support for design teams that are distributed in several locations at no extra cost.

3.2 Arasan Support Team

Our technical support is provided by the engineers who have designed the IP. That is a huge benefit for our customers, who can communicate directly with the engineers who have the deepest knowledge and domain expertise of the IP, and the standard to which it complies.

3.3 Professional Services & Customization

At Arasan Chip Systems we understand that no two Application Processors are the same. We realize that often the standard itself needs some tweaks and optimizations to fit your design better. Sometimes, the interface between the IP blocks and your design need some customization. Therefore, we provide professional services and customization to our IP customers. We do not sell our IP blocks as “black box” that cannot be touched. Please contact us for more details on our customization services.

3.4 The Arasan Porting Engine

Analog IP blocks, such as eMMC 5.1 HS400 PHY, are designed for a specific Fab and process technology. Arasan’s analog design team, utilizing its deep domain expertise and vast experience, is capable of porting the PHYs into any specific process technology required by the customer. That is “The Arasan Porting Engine”.

3.5 Pricing & Licensing

Arasan charges a one-time licensing fee, with no additional royalties. The licensing fee gives the right to use our IP for 1 project. Licensing fee for additional projects, using the same IP, is discounted. We also offer unlimited-use license. For any additional information regarding pricing and licensing – please contact our sales at: sales@arasan.com.