SLIMbus® Hardware Validation Platform

Figure 1: Photo of hardware validation platform *- Arasan's SLIMbus® Hardware Validation platform reduces development time and enables early software development.*

Features

- Compliant with MIPI® SLIMbus Specification version 1.1
- Configurable as SLIMbus Host Component as SLIMbus Active or Inactive Manager and SLIMbus Device Component as SLIMbus Inactive Manager
- GUI supports all possible configuration for an Active Manager or Inactive Manager as per SLIMbus specifications Version1.1
- GUI based interface to validate hardware using the software
- Supports all transport protocol for data transactions as per MIPI® SLIMbus Version1.0
- Enumerates all SLIMbus devices existing SLIMbus up to 256 data channel
- Reads SLIMbus device and port information
- Support for dynamic SLIMbus devices enumeration and get the device and port information
- Control space and data space channel can be configured dynamically
- During testing, GUI provides save, reload configurations and to edit existing configuration
- Simultaneously 256 data channel and control using SLIMbus massages (Activate/Deactivate, gear change, Connect/Disconnect, Multisink, and so on)
- Configures device parameters to clock gear
- GUI supports I2S Audio Interface with Mono, Stereo channel such as 2.1, 3.1, 4.1, 5.1, 6.1, 7.1 and audio support
- GUI support s SPI read and write using SLIMbus messages including user define messages
- Simultaneously transmits and receives data over multiple channel
- Resets devices, specific devices, and Host controller
- No protocol specific knowledge required
- Fully documented with required GUI picture, for example Test Scenario
- Premier support directly from engineering team
- Configures SLIMbus Host controller component on power-on reset and acts as active manager

Overview

The MIPI® (Mobile Industry Processor Interface) Alliance comprised of leading companies in the mobile industry is chartered to establish standards for hardware and software interfaces in mobile systems.

One of the MIPI® protocols is SLIMbus which provides a simple, standard, robust, scalable, low-power, high-speed, cost-effective, two wire multi-drop interface that supports a wide range of digital audio and control solutions for mobile terminals.

Arasan's SLIMbus® (Serial Low-Power Inter-chip Media protocol) analyzer provides the mobile industry a versatile tool to assist in the development and debugging of SLIMbus® products. This platform can be used by system to completely validate the implementation of the SLIMbus interface in their products during various stages of the development cycle.

Arasan Total IP Solution

Arasan Chip Systems' mobile connectivity products provide system architects and SoC design teams with silicon-proven, validated IP that helps ensure the integration and verification of digital, analog and software components in the shortest possible time with the lowest risk. These IP solutions have been incorporated into millions of mobile devices, including smart phones, tablets, digital cameras, portable game consoles, and many others.

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Arasan's high-quality Total IP Solutions include digital IP cores, analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers traffic generators, software stacks and drivers, and optional customization services for MIPI, USB, SD, SDIO, MMC/ eMMC, CF, UFS and many other popular standards.

Description

The SLIMbus Hardware Validation Platform (HVP) is a Linux-based system that can perform validation on SLIMbus Host/Device components. It can be used for SoC validation, early software development and for limited production testing. The HVP provides solutions that you need to launch your products in the shortest possible time including a binary FPGA implementation of Arasan's market leading SLIMbus Host component IP or SLIMbus Device component IP and software drivers running on a Linux OS which enables user-written programs to fully utilize the controller functions. The Arasan HVP comprises a PC platform which can run in the Fedora Linux operating system. An FPGA IP board is pre-programmed with SLIMbus Host component IP which contains SLIMbus Manager, Interface, Framer and Generic device. The DUT can either be another HVP with a complementary IP configuration or a SoC containing a SLIMbus Host component or SLIMbus Device component. The SLIMbus HVP also includes a binary version of Arasan's SLIMbus software stack. The software stack can also be used for validating SLIMbus Host/Device components during its development and integration into life cycles thereby helping designers to reduce the time to market their product.

The SLIMbus protocol specific driver stack layer implements protocols such that it can handle all SLIMbus messages and can control data transfer between different SLIMbus Components (SLIMbus Host Component to and from SLIMbus Device Component or any SLIMbus Device Component to and from any other SLIMbus Device Component) present over SLIMbus. Using Stack, we can control Active Manager of Arasan SLIMbus Host Component and can control Inactive Manager, if already any other existing Active Manager, controlling SLIMbus.

As an Active Manager, it will perform all message handling, enumerate all the devices present over SLIMbus, configure the data channel with all kinds of data transfer protocol support by SLIMbus and also can configure and control different SLIMbus component using messages.

Its supports data transfer using multiple channel between different SLIMbus devices using pushed, pulled, locked, isochronous and asynchronous protocols. It also supports functionality specific to the Arasan SLIMbus Host Component and SLIMbus Device Component IP cores. SLIMbus hardware specific driver layer is a hardware dependent layer. The layered architecture allows porting to various operating systems, various platforms and various SLIMbus® hardware devices.

Benefits

- SLIMbus Validation, Integration and Troubleshooting
- Premier direct support from Arasan IP core and software designers
- Commercial/Industrial standard test bench development platforms
- For customer, product training available

Deliverables

- Intel-based PC with Arasan SLIMbus Host Component, FPGA card with SLIMbus software stack in binary with required connecting cable and card
- HVP User Guide

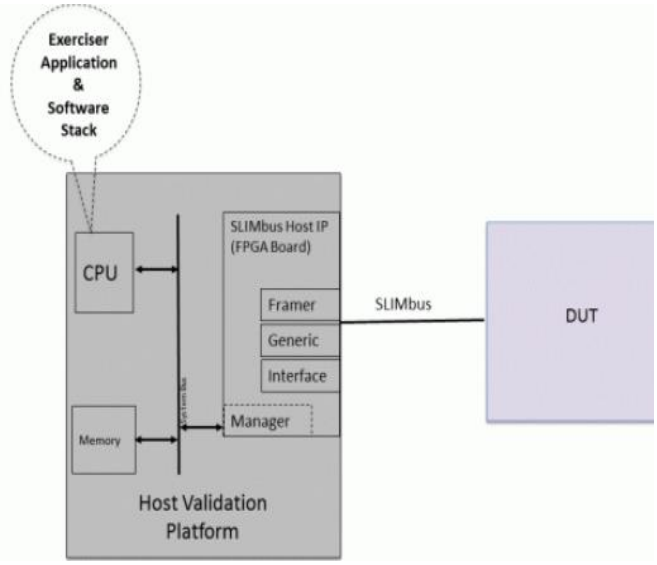

Figure 2: SLIMbus HVP Architecture

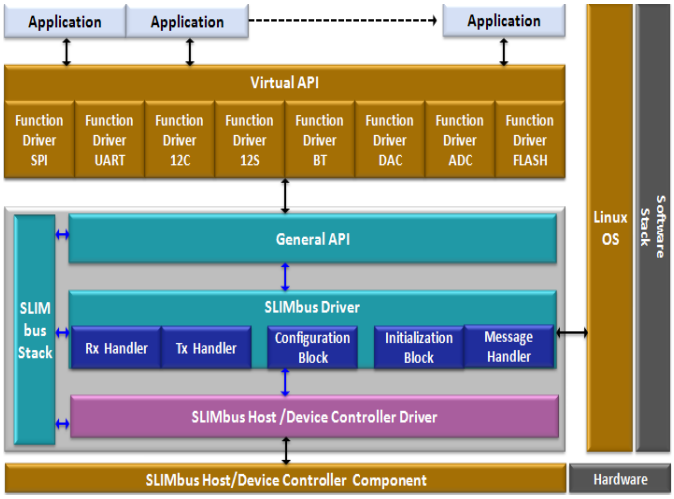

Figure 3: SLIMbus Stack Architecture

Data Sheet Links:

SLIMbus® Hardware Validation Platform:

http://arasan.com/products/hvp/slimbus/

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